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CMOS-Compatible Synthesis of Large-Area, High-Mobility Graphene by Chemical Vapor Deposition of Acetylene on Cobalt Thin Films

Michael E. Ramón,[†,‖] Aparna Gupta,[†,‖] Chris Corbet,[†] Domingo A. Ferrer,[†] Hema C. P. Movva,[†] Gary Carpenter,[‡] Luigi Colombo,[§] George Bourianoff,[⊥] Mark Doczy,[⊥] Deji Akinwande,[†] Emanuel Tutuc,[†] and Sanjay K. Banerjee[†,*]

[†]Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, United States, [‡]IBM Research, 11501 Burnet Road, Austin, Texas 78758, United States, [§]Texas Instruments Incorporated, Dallas, Texas 75243, United States, and [⊥]Intel Corporation, Austin, Texas 78746, United States. [‖]These authors contributed equally.

ABSTRACT We demonstrate the synthesis of large-area graphene on Co, a complementary metal-oxide-semiconductor (CMOS)-compatible metal, using acetylene (C_2H_2) as a precursor in a chemical vapor deposition (CVD)-based method. Cobalt films were deposited on SiO_2/Si, and the influence of Co film thickness on monolayer graphene growth was studied, based on the solubility of C in Co. The surface area coverage of monolayer graphene was observed to increase with decreasing Co film thickness. A thorough Raman spectroscopic analysis reveals that graphene films, grown on an optimized Co film thickness, are principally composed of monolayer graphene. Transport properties of monolayer graphene films were investigated by fabrication of back-gated graphene field-effect transistors (GFETs), which exhibited high hole and electron mobility of $\sim$1600 cm^2/V s and $\sim$1000 cm^2/V s, respectively, and a low trap density of $\sim 1.2 \times 10^{11}$ cm^{-2}.

KEYWORDS: graphene · acetylene · cobalt · transistor · mobility

Graphene,[1,2] an atomic thick layer of sp^2-hybridized carbon atoms bonded to one another in a hexagonal crystal lattice, is considered to be a very promising material for electronics. In particular, graphene has attracted great interest because of its unique properties, such as high intrinsic mobility,[3] thermodynamic and mechanical stability,[4] and potential for large-scale integration of ballistic carrier devices.[5] However, practical applications of graphene require high-quality, large-area graphene. Until now, mechanical exfoliation of graphite has been a primary source of graphene used for device applications. However, graphene obtained by this method is small (*e.g.*, tens of micrometers) and nonscalable.[6]

Large-area graphene films have been demonstrated by epitaxial growth on SiC substrates[7] and by chemical vapor deposition (CVD)-based methods, which involve the catalyzed decomposition of hydrocarbons on a metal surface.[8,9] A host of transition metals such as Ru,[10] Ir,[11] Cu,[8,9] and Ni[12−14] have been used as metal substrates for CVD-based graphene growth. In CVD-based growth methods, a hydrocarbon is decomposed on the metal surface, enabling graphene growth either by a combination of surface nucleation and two-dimensional growth, as in the case of Cu,[15] or by a surface segregation process of C from the metal, as in the case of Ni.[12] While having similar properties as Ni, including comparable C solubility, very limited efforts have been made so far to grow graphene on Co substrates.[16−20] In the previous reports, attempts to grow graphene on Co/SiO_2/Si were not promising since the graphene consisted of very small domains and a large fraction of the grown film was covered with multilayer graphene. In addition, there is insufficient electrical data for Co-grown graphene devices.

In this report, we present a thorough study on controlled graphene growth on Co films, using acetylene (C_2H_2) as a precursor. We also demonstrate high-mobility graphene field-effect transistors (GFETs) using Co-grown graphene films. Cobalt is an attractive substrate for graphene growth due to its distinct features, including (i) moderate C solubility ($\sim$1 atom % at 1000 °C), which might enable graphene layer thickness control by choosing the Co thickness, (ii) minimal lattice mismatch (<2%) between graphene and the Co (0001) surface, albeit only for the hcp phase at temperatures below 400 °C, (iii) easy etching and low-cost graphene transfer process, (iv) being a ferromagnetic metal, useful for spintronic

* Address correspondence to banerjee@ece.utexas.edu.

Received for review May 31, 2011 and accepted July 29, 2011.

Published online July 30, 2011
10.1021/nn202012m

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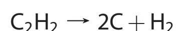
device applications, and (v) greater compatibility with Si than Cu, which is a deep trap in Si and fast diffuser, thus enabling a Si-friendly, complementary metal-oxide-semiconductor (CMOS)-compatible approach to graphene synthesis. In addition, the electronic coupling between the graphene π-states and Co d-states at the interface has been found to be quite strong compared to other transition metals.[21] C_2H_2 was chosen due to its low decomposition temperature. Back-gated GFETs were fabricated using Ni source/drain contacts to study charge transport properties. GFET transfer characteristics, as well as hole- and electron-mobility and output characteristics, are presented. Nickel contacts were chosen for their smaller contact resistivity, compared to both Ti/Au and Cr/Au, as the benefits of using graphene may be obscured by large contact resistivity.[22] Our work shows the potential for growing high-quality, large-area graphene films using Co.

RESULTS AND DISCUSSION

In our approach, graphene was grown on Co films deposited by electron-beam evaporation on SiO_2/Si substrates. In general, during metal-catalyzed growth of graphene, grain boundaries in the metal film lead to uncontrolled growth of graphene.[14] To increase the grain size, and thus reduce the number of grain boundaries, the as-deposited Co film was annealed in H_2 prior to graphene growth. Figure 1a and b show SEM micrographs of as-deposited and annealed Co films, respectively. The grain size of the as-deposited Co film was observed to be increased by annealing under an optimized flow rate of H_2 and annealing time. It was also observed that an increased flow rate of H_2 with a longer annealing time could lead to the formation of pits that impact the quality of the graphene film.

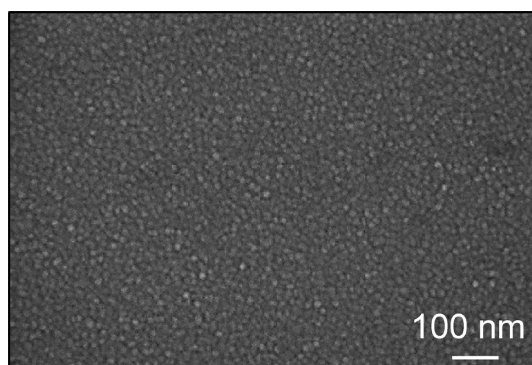
Graphene was grown on annealed Co films in a rapid thermal chemical vapor deposition (RTCVD) furnace at ~800 °C, using C_2H_2 as the carbon source. The process flow of the CVD growth of graphene on Co/SiO_2/Si, together with the possible mechanism involved, is discussed below. First, C_2H_2 molecules were adsorbed at the Co surface and catalytically decomposed into H and C atoms, according to the reaction



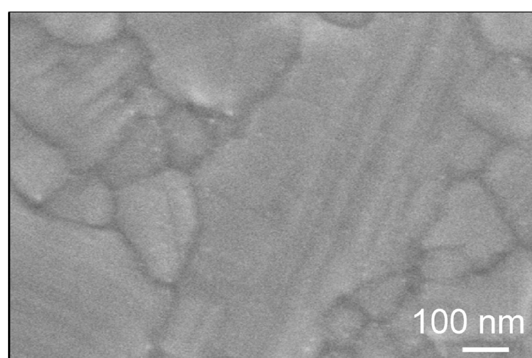
$$C_2H_2 \rightarrow 2C + H_2$$

Hydrogen was then desorbed from the surface, leaving C atoms to dissolve into the metal film. The solubility of C in the Co film is moderately high (~0.4 atom %) at the growth temperature (~800 °C) and decreases upon cooling, leading to the segregation of C atoms out from the Co film to the surface, forming a continuous film of graphene. After growth, the graphene was transferred to another SiO_2/Si substrate and characterized by optical microscopy[23] and Raman spectroscopy.[24]

The influence of the thickness of the Co film on the quality of graphene was investigated by comparing the optical micrographs of graphene grown on 100, 200, and 300 nm Co films, as shown in Figure 2a−c, respectively. The lightest pink region, as indicated in Figure 2a, corresponds to monolayer graphene, covering ~80% of the area shown. The second lightest pink and the darker regions in Figure 2a exhibit bilayer and multilayer graphene/few-layer graphene (FLG), respectively. Two distinct features are inferred from the color contrast of the optical images: (i) the surface area coverage of monolayer graphene decreases with the increase in Co film thickness, as shown in Figure 2d, and (ii) the formation of multilayer graphene regions with smaller domain size increases with the thickness of Co film. This is expected since the amount of C dissolution in the metal and subsequent segregation to the surface depends on the thickness of the metal layer. Thinner films are saturated with a fewer number of C atoms; consequently, the reduction of the temperature during the cooling process leads to the formation of monolayer graphene, suppressing multilayer growth. Increase of the Co film thickness allows more C atoms to be dissolved, and during cooling, the excess C atoms segregate to form multilayer graphene, as shown in Figure 2b and c. These results are similar to graphene growth on Ni films and indicate that graphene growth on Co takes place through a surface segregation process.[25]



(a)



(b)

Figure 1. SEM images of Co film (a) before and (b) after annealing, showing increased Co grain size.

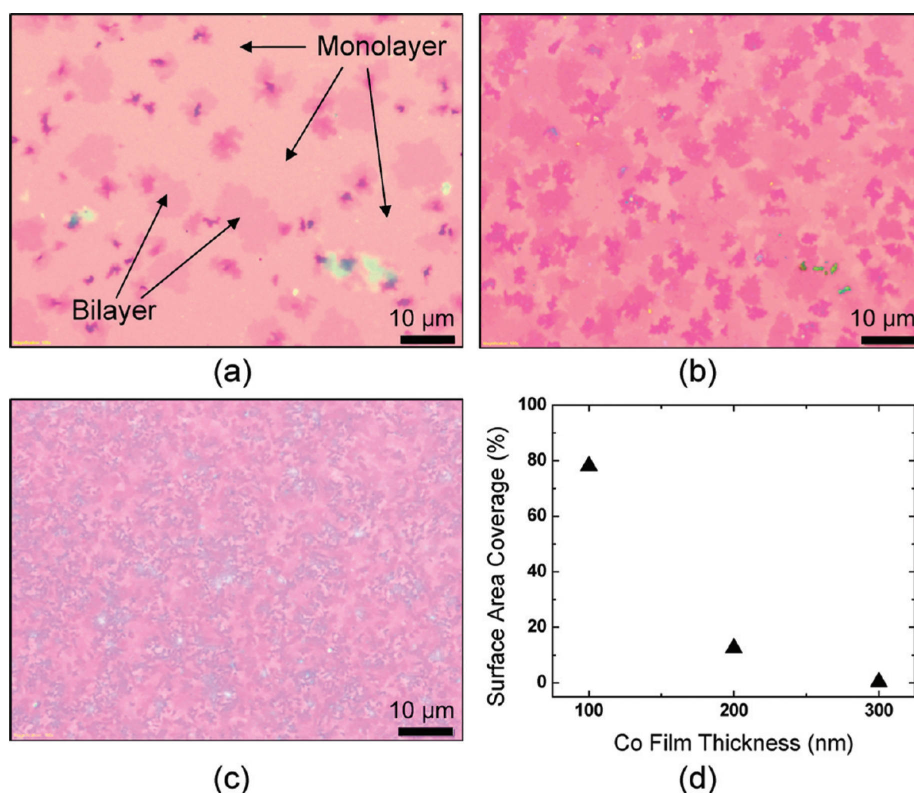


Figure 2. (a) Optical micrographs of graphene grown on (a) 100 nm Co film, showing large monolayer area along with small domains of bi- and multilayer area, and (b) 200 nm and (c) 300 nm Co films. All scale bars are 10 μm. (d) Percentage surface area coverage by monolayer graphene as a function of Co film thickness.

On the basis of these results, a thinner (<100 nm) Co film could be expected to promote better monolayer graphene growth as the number of C atoms dissolved into the Co film at the growth temperature (800 °C) and subsequent segregation of C atoms upon cooling would be less. However, we have observed that thinner Co films (~60 nm) agglomerate at the growth temperature (800 °C), forming pits (see Supporting Information, Figure S1), which leads to poor graphene quality. The agglomeration also appears at higher temperature (900 °C) for optimized Co film thickness (100 nm) (see Supporting Information, Figure S2).

Raman spectroscopy was used to further evaluate the thickness, quality, and uniformity of the graphene films, as shown in Figure 3. The optical micrograph is displayed in Figure 3a, showing a selected area of 35 μm × 30 μm, which was investigated thoroughly using Raman mapping. Figure 3b and c show the color map of 2D peak intensity and the Raman spectra taken from the regions, marked with the corresponding colored circles, respectively. The Raman spectrum corresponding to the black-circled (pink-circled) region shows a 2D peak position at 2675 cm^{-1} (2675 cm^{-1}) with a full width at half-maximum (fwhm) of ~29 cm^{-1} (~30.5 cm^{-1}) and I_{2D}/I_G of ~3.89 (~3.1), indicating monolayer graphene.[9,26] In contrast, the Raman spectrum associated with the green-circled (blue-circled) region yields a 2D peak position at 2688 cm^{-1} (2695 cm^{-1}), a fwhm of ~35 cm^{-1} (~42 cm^{-1}), and I_{2D}/I_G of ~1 (~1), which reveals the formation of bilayer (multilayer) graphene.[9,17] However, the fwhm of the 2D band and the 2D-to-G intensity ratio of the Raman spectrum, taken from the multilayer region, clearly imply that the number of associated graphene layers does not exceed 5. A blue shift of the 2D peak position with the increase of number of graphene layers was observed by normalizing the 2D bands, as shown in Figure 3d. This is consistent with the previous report on exfoliated graphene films.[27] The number of layers was further verified from Raman mapping, corresponding to the fwhm of the 2D band, as displayed in Figure 3e. The lower limit in the color range in Figure 3e represents a fwhm = 26 cm^{-1}, while the upper limit corresponds to a fwhm = 58 cm^{-1}. Figure 3e strongly supports that most of the mapped area of the film (~95%) consists of monolayer graphene, having a fwhm less than 33 cm^{-1}, with only a small fraction corresponding to possibly bilayer and multilayer graphene.[9] In addition, Raman mapping corresponding to the intensity of the G-band (Figure 3f) further validates the uniformity of the film as consisting of predominantly monolayer graphene. D-bands, associated with the defects and/or disordered carbon atoms, were also observed at around 1340–1350 cm^{-1} in the Raman spectra. As shown in Figure 3c, the D-to-G peak intensity ratio becomes smaller with the increase in number of graphene layers. This may be due to lattice strain predominantly affecting the first graphene

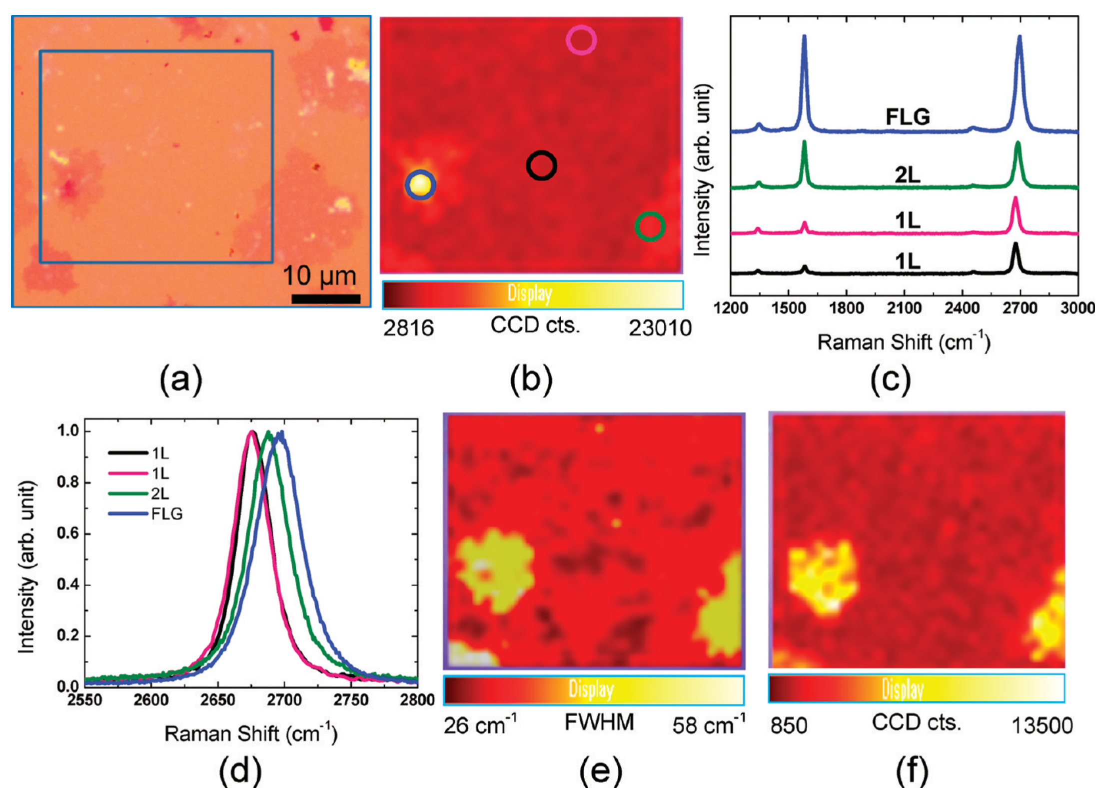


Figure 3. (a) Optical micrograph of graphene film transferred onto SiO_2/Si. (b) Raman mapping image of 2D band intensity within the area marked in (a), showing large-area monolayer graphene with a small fraction of bilayer and multilayer/few-layer graphene (FLG). (c) Corresponding Raman spectra of the circled regions in (b). Raman spectra corresponding to the black-circled and pink-circled regions indicate monolayer graphene with 2D peak positions at 2675 cm^{-1}. Raman spectra associated with the green-circled and blue-circled regions indicate bilayer and multilayer graphene/FLG with 2D peak positions at 2688 and 2695 cm^{-1}, respectively. (d) Normalized 2D peak intensities corresponding to the Raman spectra in (c), showing a blue shift of the 2D peak position with the increase of number of graphene layers. (e) Raman mapping of 2D band peak width and (f) G band intensity in the same region mapped in (b).

layer attached to the Co surface during growth or to the wet etching process to remove the underlying Co film during transfer of the graphene layer to the SiO_2/Si substrate.[17] The second reason is more likely in our case, as we observed negligible D-band in the graphene films before transfer. In addition, we cannot avoid the possibility of dangling bonds on the graphene film after removing the Co film, which may introduce more defects in the graphene film, thereby increasing the D-band intensity.

Transport properties of Co-grown graphene films were studied by fabricating back-gated GFETs with Ni source/drain contacts on monolayer regions of transferred graphene films by using electron beam lithography (EBL). The inset in Figure 4b shows an example optical microscope image of a fabricated device. From the transfer characteristics (Figure 4a), we observe an I_{ON}/I_{OFF} ratio of ~3, which is comparable to other reported devices fabricated by CVD growth on Cu.[6,15] The minimum conductivity (maximum resistivity) point observed in the transfer characteristics (four-point resistance ($R_{4\text{-Point}}$) versus $V_{BG} - V_{DIRAC}$) as shown in Figure 4a and b, respectively, corresponds to the charge neutrality point (known as the Dirac point), indicating an equal concentration of holes and electrons. We observed positive Dirac points in our devices, which may be due to unintentional extrinsic hole-doping caused by adsorbants that were introduced during device processing.[6,28,29]

Hysteresis, as indicated by the shift in the Dirac point between forward and reverse sweeps of the back-gate voltage, V_{BG}, was observed to be ~3 V (Figure 4a), indicating the presence of trapped charges at the SiO_2/graphene interface.[30] These trapped charges may be introduced, to a certain extent, by the Co etching and transfer process, as previously described. The number of trapped charges per unit area N (*i.e.*, charged impurities) can be estimated from the shift in the Dirac point and the oxide capacitance (C_{ox}) of the SiO_2 bottom dielectric as $N = C_{ox}\Delta V_{DIRAC}/2e$.[31] From this equation, we calculate N to be $\sim 1.2 \times 10^{11}$ cm^{-2}, where C_{ox} is ~12 nF/cm^2. This value of trapped charge is low and in good agreement with previous studies[31−33] and, despite the possibility of unintentional doping during device fabrication, is indicative of a relatively clean sample.[33]

Mobility was calculated by fitting the measured $R_{4\text{-Point}}$ *versus* $V_{BG} - V_{DIRAC}$ data to the model for GFET resistance described elsewhere.[34] In particular, we have compared electron and hole mobility for our devices. Specifically, as shown in Figure 4b, the data were separately fit for holes, $V_{BG} - V_{DIRAC} < 0$, and for

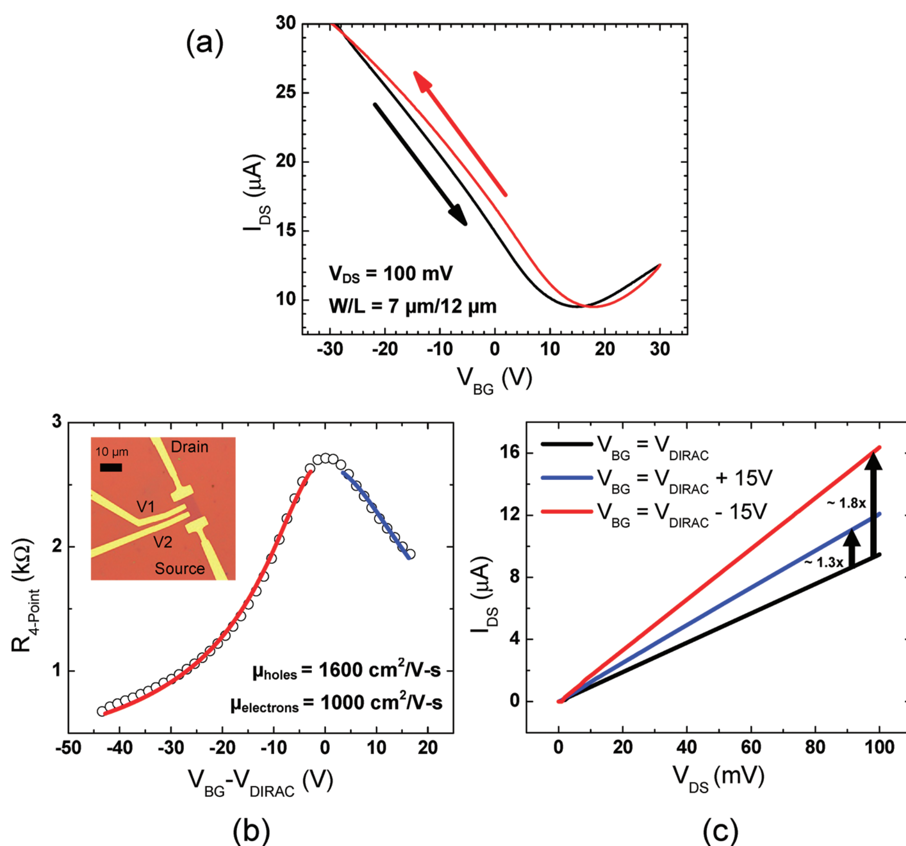


Figure 4. (a) GFET transfer characteristics. From the hysteresis, the number of trapped charges per unit area was found to be $\sim 1.2 \times 10^{11}$ cm^{-2}. (b) $R_{4\text{-Point}}$ versus $V_{BG} - V_{DIRAC}$ and extracted hole and electron mobility, indicating preferential hole conduction over electron conduction. Inset: Optical microscope image of a 4-point GFET. (c) Output characteristics at $V_{BG} = V_{DIRAC}$ (black), $V_{BG} = V_{DIRAC} - 15$ V (red), $V_{BG} = V_{DIRAC} + 15$ V (blue). Drain current modulation is much greater when the graphene is electrostatically doped p-type ($V_{BG} - V_{DIRAC} < 0$), as compared to when the graphene is comparably electrostatically doped n-type ($V_{BG} - V_{DIRAC} > 0$), which is expected given the higher mobility for holes as compared to electrons (b).

electrons, $V_{BG} - V_{DIRAC} > 0$. The resulting mobility was $\sim$1600 cm^2/V s for holes and $\sim$1000 cm^2/V s for electrons, indicating preferential hole conduction over electron conduction, which may be due in part to the unintentional extrinsic doping.[28,29] Such preferential hole conduction has been reported for various sources of graphene, including graphene synthesized by CVD over Cu.[6] From the $R_{4\text{-Point}}$ *versus* $V_{BG} - V_{DIRAC}$ data of Figure 4b, and complementary $R_{2\text{-Point}}$ *versus* $V_{BG} - V_{DIRAC}$ data measured on the same device, we extracted a 4-point to 2-point mobility ratio ($\mu_{4\text{-Point}}/\mu_{2\text{-Point}}$) of $\sim$1.5 and a contact resistivity ρ_C of $\sim$2135 Ω μm, where $\rho_C = R_{contact}W = (\sim 300\ \Omega)(7\ \mu\text{m})$. These results are in excellent agreement with previous results[22] and imply that the contact resistivity is characterized by the channel width as opposed to the contact area.

As further confirmation of the preferential hole conduction over electron conduction in our GFETs, Figure 4c shows the output characteristics for holes and for electrons at various values of V_{BG}. No current saturation is observed over the range of V_{DS} from 0 V to 100 mV. As shown, the modulation of the drain current is much more significant when the graphene is electrostatically doped p-type ($V_{BG} - V_{DIRAC} < 0$), as compared to when the graphene is comparably electrostatically doped n-type ($V_{BG} - V_{DIRAC} > 0$). This is expected given the higher mobility for holes observed in our devices (Figure 4b). Indeed, the I_{DS} at $V_{DS} = 100$ mV for $V_{BG} - V_{DIRAC} = -15$ V is $\sim$1.8 times greater than the I_{DS} at $V_{BG} = V_{DIRAC}$, while the I_{DS} at $V_{DS} = 100$ mV for $V_{BG} - V_{DIRAC} = +15$ V is $\sim$1.3 times higher than the I_{DS} at $V_{BG} = V_{DIRAC}$.

CONCLUSION

In summary, we have grown large-area monolayer graphene films on Co films deposited on SiO_2/Si substrates by a CVD-based process using C_2H_2 as a carbon source. The number of graphene layers is influenced by the Co film thickness. Raman spectra and mapping show that our graphene films are predominantly monolayer ($\sim$80% monolayer surface coverage). Moreover, by performing a thorough analysis of the 2D fwhm, 2D peak position, and the 2D-to-G intensity ratio, we have characterized the nature of monolayer graphene, as compared to bilayer and multilayer graphene/FLG. Electrical transport measurements reveal high mobility values

of ~1600 and ~1000 cm^2/V s for holes and electrons, respectively. Our GFETs also exhibited an I_{ON}/I_{OFF} ratio of ~3 and low trap density of ~1.2×10^{11} cm^{-2}. These results show the promise of using Co for monolayer graphene synthesis, which could be useful for Si-based, CMOS-compatible nanoelectronics.

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MATERIALS AND METHODS

Graphene Growth and Transfer. A 285 nm thick SiO_2 layer was grown by thermal dry oxidation on a Si (100) substrate, followed by e-beam evaporation of 100−300 nm thick Co films. An RTCVD furnace was used for graphene synthesis, using C_2H_2 as the carbon source. The base pressure of the growth chamber was ~1.5×10^{-8} Torr. At the beginning of the RTCVD process, the Co film was annealed in H_2 at ~650−700 °C for approximately 10 min to increase grain size, followed by elevation to the growth temperature of ~800 °C and insertion of C_2H_2 into the growth chamber. The sample was held at the growth temperature for 1−2 min. After completion of the C_2H_2/H_2 flow process step, the sample was rapidly cooled in a H_2 atmosphere to room temperature. After growth, the graphene/Co surface was spin-coated with a poly(methyl methacrylate) (PMMA) support layer, and the Co was etched away in a solution of ferric chloride ($FeCl_3$). The graphene was then transferred to another SiO_2/Si substrate, after which the PMMA support layer was dissolved in acetone.

Physical Characterization. The Co and graphene films were investigated using optical microscopy (Olympus BX51M), scanning electron microscopy (SEM: ZEISS Neon 40), and Raman spectroscopy (Renishaw inVia Raman microscope) using a 532 nm excitation wavelength.

Transistor Fabrication and Electrical Characterization. Graphene films were transferred to an arsenic-doped Si (100) substrate with a very low resistivity of less than 5 mOhm cm, upon which a 285 nm thick SiO_2 layer was grown by thermal dry oxidation. The low resistivity Si substrate allows for its use as a global backgate. Monolayer graphene regions used for device fabrication were identified and selected by a combination of optical microscopy and Raman spectroscopy. An active region was defined by EBL and oxygen plasma etching. A second EBL step was performed to define metal contacts for a four-point structure, followed by a 50 nm thick Ni e-beam evaporation and liftoff process. All electrical measurements were taken on similar back-gated devices at room temperature in a vacuum probe station using an Agilent 4156C semiconductor parameter analyzer.

Acknowledgment. This work is supported by NRI-SWAN and by DARPA Contract FA8650-08-C-7838 through the CERA program and IBM-UT Subcontract Agreement W0853811. M.R. also gratefully acknowledges funding from the Robert Noyce Memorial Fellowship, the Cockrell School of Engineering Fellowship, and NSF-IGERT Grant No. DGE-0549417.

Supporting Information Available: SEM and optical microscopy images show results obtained for thinner Co films (~60 nm), as well as results at higher temperature (900 °C) for the optimized Co film thickness (100 nm). This material is available free of charge *via* the Internet at http://pubs.acs.org.

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